TECHNIQUES FOR SEQUENTIALLY TRANSFERRING DATA FROM A MEMORY DEVICE THROUGH A PARALLEL INTERFACE

ABSTRACT OF THE DISCLOSURE

[0067] Techniques are provided for synchronously transmitting data in parallel from an external memory device to a destination circuit using a sequential read mode. The memory device includes an address counter. The address counter generates sequential read addresses for the data bits stored in the memory device. The destination circuit generates a clock signal that controls the address counter. The destination circuit can also transmit a start address to the memory device. The address counter sequentially generates a new read address in response to transitions in the clock signal beginning with the start address. Data bits are transferred in parallel from the memory device to the destination circuit.

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